Section I - Clean Version

The Pending Claims:

1. An integrated circuit device comprising:

a conductive pad to receive an input signal from an external signal line;

a first doped region of first conductivity type disposed in a semiconductor substrate of second conductivity type, underlying and surrounding the conductive pad;

a conductive region of first conductivity type disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

2. The integrated circuit device of claim 1 wherein the first and second supply voltages are ground.

3. The integrated circuit device of claim 2 wherein the first tap region completely surrounds the first doped region.

4. The integrated circuit device of claim 1 wherein the first tap region is a discontinuous region.

5. The integrated circuit device of claim 1 wherein the doping concentration of the first doped region is less than the doping concentration of the conductive region.

6. The integrated circuit device of claim 1 wherein the first tap region is a third doped region and the second tap region is a fourth doped region.

7. The integrated circuit device of claim 6 wherein the third doped region is of an opposite conductivity type than the first doped region.

8. The integrated circuit device of claim 6 wherein the fourth doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

9. The integrated circuit device of claim 1 wherein a portion of the first tap region is decoupled from the first supply voltage to provide a predetermined equivalent series resistance between the first doped region and the first supply voltage.

10. The integrated circuit device of claim 5 wherein the first tap region substantially surrounds the first doped region.

11. The integrated circuit device of claim 10 wherein the first tap region is a discontinuous region.

12. A bond pad for an integrated circuit device, the bond pad comprising:

a conductive bonding layer;

a first doped region of first conductivity type formed in a semiconductor substrate of second conductivity type, underlying and surrounding the conductive bonding layer;

a conductive region of first conductivity type disposed in the first doped region, the conductive region having a surface area at least substantially equal to the surface area of the conductive bonding layer; and

a conductive tap region spaced apart from and surrounding at least a portion of the first doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

13. The bond pad of claim 12 wherein the supply voltage is a ground voltage and the conductive bonding layer includes a metal.

14. The bond pad of claim 12 wherein the doping concentration of the first doped region is less than the doping concentration of the conductive region.

15. The bond pad of claim 12 wherein the conductive tap region is a third doped region and is of an opposite conductivity type than the first doped region.

16. The bond pad of claim 12 wherein a portion of the conductive tap region is decoupled from the supply voltage to provide a predetermined equivalent series resistance between the doped region and the supply voltage.

17. The bond pad of claim 12 wherein the conductive tap region is a continuous region.

18. The bond pad of claim 17 wherein the conductive tap region substantially surrounds the doped region.

19. The bond pad of claim 12 wherein the conductive tap region is a discontinuous region.

20. The bond pad of claim 19 wherein the conductive tap region substantially surrounds the doped region in a concentric-like manner.

21. The bond pad of claim 12 wherein the conductive region is polysilicon.

22. The bond pad of claim 21 wherein the conductive tap region is an doped layer positioned beneath the conductive region.

23. A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:

a drain region of first conductivity type formed in a semiconductor substrate of second conductivity type, the drain region being electrically coupled to the bond pad;

a source region of second conductivity type; and

a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region.

24. The transistor layout of claim 23 wherein the supply voltage is coupled to a ground voltage.

26. The transistor layout of claim 23 wherein the conductive tap region is spaced proximal to and completely surrounds the drain region.

27. The transistor layout of claim 23 wherein the conductive tap region is a discontinuous region.

28. The transistor layout of claim 23 further including:

a plurality of source regions, each source region of the plurality of source regions being electrically and physically coupled to the conductive tap region;

a plurality of drain regions, each drain region of the plurality of drain regions being electrically coupled to the bond pad; and

wherein the conductive tap region is spaced proximal to and surrounds at least one drain region of the plurality of drain regions.